

Multicore Computer Architecture - Storage and Interconnects

Tutorial 4

Main Memory Concepts



NPTEL Online Course: Multi-Core Computer Architecture and Interconnects, Dr. John Jose, IIT Guwahati

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Tutorial Problem-1

- ❖ Consider a system that uses 24 bit virtual address space and 20 bit physical address space. It uses a paging scheme that employs 4KB pages. The page table for a program is indexed based on virtual page number and each entry contains the frame number and 8 control bits. What is the size of the page table in bytes?

Tutorial Problem-2

- ❖ A 32 GB DRAM system that uses 4 channels (C0, C1, C2 and C3) has 4096 columns per row. It uses 8B wide memory bus to transfer data from DRAM to the processor. If adjacent memory words are mapped on to adjacent memory channels, which channel will fetch the physical address 0x 3488A742?

Tutorial Problem-3

- ❖ Consider a 64 GB DRAM system organized as 4 channels, each channel with 2 DIMMs, each DIMM having 2 ranks. The system uses 8 bit chips and 8 banks. Each bank has a collection of byte-cells (can store 8 bit of information) organized as rows and columns. ie, the meeting point of a row and column is a byte cell. The bank configuration is in such a way that the number of rows and columns per bank is equal. The system uses 8 byte wide memory bus to transfer data from DRAM to the controller. Each channel is connected to 16GB of continuous memory.
- ❖ What is the total number of columns per bank?
- ❖ What is the total number of rows in the entire DRAM system?

Tutorial Problem-3 contd..

- ❖ If the system is using row interleaving in banking, which bank the physical address 0x 844332255 is mapped to? Which channel serves data belonging to this address?
- ❖ If the system uses a 128B last level cache and is using cache block interleaving in banking, which bank the physical address 0x 2244668AA is mapped to? Which channel serves data belonging to this address?

Tutorial Problem-4

- ❖ In a DRAM system that follows open row buffer management policy, which of the following sequence of commands are generated if the new request is to a different row from the row that was accessed last?
 - (A) Activate
 - (B) Precharge
 - (C) Activate followed by Precharge
 - (D) Precharge followed by Activate

Tutorial Problem-5

- ❖ For a sequence of memory requests coming to a particular bank at regular intervals such that every request reaches the scheduler when the processing of the previous request is in progress, which of the following holds true for FR-FCFS scheduler?
- A. Open page policy gives lesser average turnaround time than closed page policy.
 - B. Closed page policy gives lesser average turnaround time than open page policy.
 - C. Closed page policy gives less average starvation than open page policy.
 - D. Both open and closed page policy gives same average turnaround time.
 - E. Cannot be compared with the given details.

**THANK
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